

Research Needs for Novel Devices

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Introduction

The ITRS roadmap for the semiconductor industry predicts that conventional CMOS technology will be extended until 2016 and the 22 nm node before scaling will slow down or stop. Prior to that time, there are a huge number of difficult technological challenges that must be met and overcome. The ITRS roadmap document identifies, organizes and synchronizes the technology needs so it is reasonably clear what needs to be done although it is far from clear how it is to be done. A companion document to this goes one step further and prioritizes those needs to help focus the SRC research effort and optimize the research program in this area.

The technological challenges for the information processing industry in the post CMOS era are quite different because it is far from clear what needs to be done. There is a growing consensus that from about 2016 forward, the information processing technology will consist of a heterogeneous set of novel and widely disparate technologies integrated on a silicon platform consisting of very fast, very small and very cheap CMOS devices. These novel devices will span a very broad range of materials, operational principles, functionalities, logic systems, data representations and architectures. In general, their characteristics will be complimentary to scaled CMOS and none of the technologies currently on the horizon has any real possibility of replacing silicon.

The vast reach and scope of the technical options that populate the post CMOS technology space make structuring a finite size research program an intimidating task. It is very difficult to formulate a metric that will enable comparisons of widely different devices functioning in different architectures on different applications. One objective of this document is to provide a structure or taxonomy that will help prospective proposers understand where various technologies fit, what are the competitive approaches and what are the relevant figures of merit.

During the last several years there has been a huge amount of government-sponsored research loosely described as nanotechnology. This effort has lacked organization and direction and consequently is of little immediate value to the semiconductor industry. However, the associated body of knowledge provides a rich resource that can be used as a starting point for targeted research programs such as this. Proposals that build on previously funded nanotechnology will in general be well leveraged and will be looked on favorably.

The occasion for this report is the upcoming call for proposals in Novel Device Technologies to be issued in early 2003. The proposals selected will form a continuation of the Novel Device Technology program initiated in 2000 and will extend for 3 years. The intent of the SRC is to create a very long range, far reaching program of research that will enable successful introduction of new technologies for the post CMOS era. This document will describe the overall scope of that program and attempt to prioritize the research needs.

The organization of this document is taxonomy of post CMOS devices followed by brief descriptions of each of the major categories arranged according to state variable. As with any taxonomy, some issues

will apply to multiple categories and these will be defined as crosscut issues and prioritized separately. The research needs associated with each of the major categories will be summarized in a table at the end of the document and ranked according to research need, research gap and leverage potential. These ranking metrics will be defined more fully in the research needs section. The overall objective of this document is to provide guidance to the university research community concerning research needs and priorities relating to the novel device program solicitation.

Representatives of SRC member companies engaged in long-range research have written this report. The authors and company affiliations of this report are shown below.

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1. Taxonomy and organization

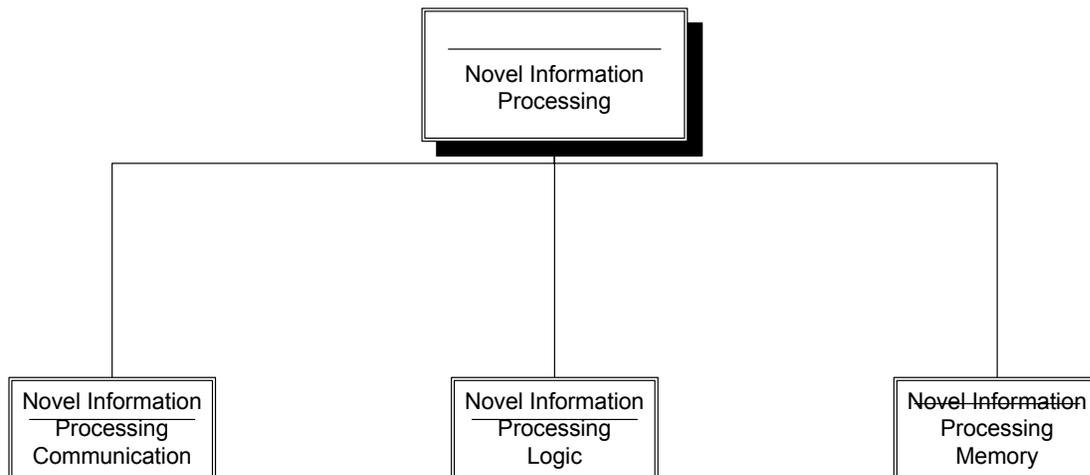
As mentioned in the introduction, the domain covered by post CMOS information processing devices is so broad that it is absolutely essential to introduce a natural taxonomy to the field to enable a rational research program. The committee spent a substantial amount of time discussing the organization of the report before any technical details were ever encountered and created the taxonomy described below.

Application/state variable/device

The committee decided that a top down, hierarchal organization was required and that the highest level in the hierarchy would be the application. We felt that information processing could be categorized into three principle applications – logic, memory and communication as shown in figure 1.

Figure 1 Top-level information processing categories

The second level in the information processing taxonomy is the state variable used to define the computational state. This concept requires further description.



For the last 40 years, CMOS information processing devices and architectures have uniformly used the presence or absence of electric charge and current to define computational state. Prior to that, information processing has used other physical embodiments of computational state including ferromagnetic orientation in ferrite-based memories, holes in paper tapes and punch cards and even beads on a string. In the future, it will be necessary to utilize other physical representations of computational state to achieve substantial performance improvements beyond that achievable with scaled CMOS. Alternative devices and architectures utilizing alternative representations of computational state are already fairly common in the research environment. However, no systematic indexing of these devices according to state variable has been undertaken.

The committee decided to include the 8 state variables in the novel information processing taxonomy listed below and to organize the report around these state variables.

- Electric charge
- Molecular state
- Spin orientation
- Electric dipole orientation
- Photon intensity
- Quantum state
- Phase state
- Mechanical state

White papers submitted in response to this solicitation are requested to classify themselves according to the taxonomy outlined above.

2. Relevance criteria

Post CMOS devices span multiple applications, state variables and technologies and are extremely diverse in nature and defining a common figure of merit that can be applied to every alternative technology is extremely challenging. One way to approach the task is to define a set of nanotechnology relevance conditions that parameterize how applicable a given technology is to information processing applications. Novel technologies may then be compared based on how well they rate using the following set of relevance conditions. White papers submitted in response to this solicitation are requested to address each of the relevance conditions below as quantitatively as possible.

Energy efficiency

Energy efficiency appears likely to be the limiting factor of any post CMOS device using electric charge or electric current as a state variable. It also appears likely that it will be dominant criteria in determining the ultimate applicability of alternate state variable devices.

CMOS compatibility

The semiconductor industry has been based for the last 40 years on incremental scaling of device dimensions to achieve performance gains. The principle economic benefit of such an approach is it allows the industry to fully apply previous technology investments to future products. Any alternative technology will need to utilize the tremendous investment in infrastructure to the highest degree possible.

Performance

Future performance metrics will be very similar to current performance metrics. They are cost, size, speed and energy dissipation.

Scalability

In order to derive the economic benefit of incrementalism mentioned above, any alternative technology should be scalable through multiple generations. It will be desirable to make incremental modifications to the alternative technology and achieve integer multiples of performance. In other words, it should be possible to articulate a Moore's law for the proposed technology.

Architectural compatibility

This criteria is motivated by the same set of concerns that motivate the CMOS compatibility, namely the ability to utilize the existing CMOS infrastructure that currently exists. The architectural compatibility is defined in terms of the logic system and data representation used by the alternative technology. CMOS utilizes Boolean logic and a binary data representation and ideally, the alternative technology would need to do so as well.

Sensitivity to parametric variation

As devices approach the atomic scale, they become very sensitive to manufacturing and environmental variations. Thus parametric sensitivity is an important criterion for evaluation of alternative technologies. The goal should be a device that is affected but not dominated by parametric variations.

Room temperature operation

Room temperature operation is desirable because advanced cooling systems can add tremendously to the cost.

Stability and reliability

As devices approach the atomic scale, structural compositional stability to thermal fluctuations becomes a significant concern. Any realistic alternative device must show structural stability at room temperature for at least 7 years.

3. State variables for information processing

The following discussions describe the eight alternative state variables currently in use or being proposed by the research community. Each segment contains a brief physical description of the alternative data representation, a few examples devices and the critical research needs associated with that state variable.

A. Electric charge

For the last four decades, most of the information processing devices relied on electric charge as state variables. The CMOS device is the representative technology that utilized the electric state variable. There are many attempts trying to challenge the dominant role of CMOS technology. They all fall short because of the outstanding rate of progress in silicon CMOS technology. It is therefore important to evaluate any post CMOS device option that can provide substantial benefits compared to extreme scaled CMOS devices. We will consider three representative examples: nanotubes, quantum wires/dots, and molecular devices, all of which use electronic charge to define computational state.

Nanotubes

The nanotubes are unique nanostructures with interesting electrical, mechanical, thermal, and optical properties. Its electronic properties depend on structural parameters such as diameter, helicity, location and type of defect. Although carbon nanotube FETs and circuits have already been demonstrated, the conductance mechanism through the nanotubes as well as the contact is not yet well understood. To ensure scalability, the electrostatic properties of an individual nanotube as well as an array of nanotubes

must be explored. It's not clear what will limit the size of a nanotube-based system. Will it be the size of tubes or the cross talk between nanotubes? In order to drive long interconnected wires, multiple single-wall carbon nanotubes are needed to provide enough drive current. The effective width of the device is no longer a continuous function. The impact of this discrete width effect on circuit and system design should be evaluated. The fabrication method of growing or placing nanotubes in a controlled manner is still far from acceptable. Circuit redundancy technique may be needed to handle this variation issues. Mechanical properties of CNTs that are used to define mechanical state of devices, are discussed in the next steps.

Quantum Devices

Devices that explore the quantum size effects such as quantum dots and quantum wires have been proposed for logic and memory applications. However the severe random background charge effect has prevented these devices for any practical applications. Moreover, the drive current for this type of devices is generally poor. This limits the speed of the system due to insufficient drivability. The critical dimensions for these devices must be very small. Traditional lithography cannot be used to fabricate these devices. Some sort of self-assembly nanofabrication technique is inevitable. While the self-assembly technique can control variation in a localized scale, the variations in a global scale in any self-assembly process is still relatively large. In order to utilize this type of devices, unconventional circuit and system architectures are needed to circumvent the above problems.

Molecular devices

There are many interesting proposals for molecular devices. One exciting idea is to use the nature of molecular chemistry to define the channel of a FET by scaling transistors all the way to the molecular level. The electrostatic and transport properties of a molecular device depend on the particular molecule used. How to custom make molecular FET is still an open question. Some sort of self-assembly process will most likely be required. An opportunity exists to explore the interplay between the processes, integration and the system design of these molecular devices.

Research needs

- Fabrication and control of CNT material properties
- Design impact of quantized device characteristics
- Uniformity of self assembled quantum structures
- Low drive currents of quantum devices

B. Mechanical state

So far, the research world in the novel device arena has focused much of its effort on novel, bottom-up approaches to advanced functional devices. As such, most of the research on nanotubes, nanowires and other novel materials has concentrated on the use of these structures for use as elements in field effect transistors and logic gates. Much less attention has been given to devices that take advantage of mechanical, electromechanical and highly perfect structural properties, of materials like nanotubes/nanowires, or materials that can represent 'state' through a physical change. Below are some examples of devices that exhibit states through mechanical means, and some of the research needs still to be addressed. These examples illustrate a great advantage of mechanical systems in that they are generally simplistic in concept, and there is a large existing infrastructure in the 'micro scale' to draw experience and expertise from. The problems of mechanical devices are that they generally have issues of fatigue, wear and hence lifetime. Additionally, anything that moves, or changes shape, must have compliant materials to account for the movement/shape change.

Nanotube Switching Devices

The mechanical properties of CNT are very attractive for use as NEMS devices.

- Very high Young's modulus of 1.2 TPa (silicon is about 170GPa)
- Low density of 1.33 g/cm³ (Silicon ρ = 2.33 g/cm³)

- Amazing tensile strength (1000 X steel)
- Structural perfection (giving high Q and low loss) – Si and GaAs begin to have serious problems when the beams thinned down to the nm sizes needed for high frequency switch or resonator structures. CNT are a single molecule, and grow perfectly.
- CMOS compatible (demonstrated by both Infineon and Stanford University)

Possible applications include:

- switch
- memory
- sensors, transducers
- resonators

Research needs for nanotube and nanowire switches

- Fatigue and failure modes of CNTs under 10^{17} operations
- Low resistance, high reliability contacts to the 1D-structures
- Developing methodologies to induce nanotube and nanowire deflections.
- Develop an understanding of tube transport variation with applied mechanical deformations

Nanotube resonator devices

Brief calculations to determine the resonant frequency range of CNTs and consequently their applicability in high frequency (above 500 MHz) MEMS resonator applications have shown that a single-walled nanotubes (diameter of 1.4 nm), in a clamped-clamped 1 micron MEMS resonator configuration would have a fundamental mode resonance at only approximately 36 MHz. Research on MWCNTs, and smaller beam sizes for true RF frequency devices would be useful.

Phase Change Memories

Ovonic Unified Memory (OUM) is a memory technology, originally developed by Energy Conversion Devices. (ECD), and licensed to Ovonyx, Inc. OUM uses a reversible structural phase-change --from amorphous to a crystalline phase -- and the associated resistance change in a thin-film chalcogenide alloy material ($\text{Ge}_2\text{Sb}_2\text{Te}_5$).

The active material acts as a programmable resistor, switching between high (amorphous) and low (polyX'tal) resistance in ~nanosec. timescale. Information stored in the cell is read out by measurement of the cell's resistance. This technology can be integrated in the backend of current CMOS process.

Phase change memories are, non-volatile, have the capability to be high density, exhibit high endurance – ($>10^{13}$), have a high switching speed, have non-destructive reads, direct overwrite capability, and no charge loss failure mechanisms.

OUM is not a perfect memory, but, <100 nsec write performance is 'good enough' for many portable applications, could be cheaper than MRAM & FeRAM and the phase change materials ($\text{Ge}_2\text{Sb}_2\text{Te}_5$) are currently in production for optically rewritable disks.

Research Needs

- OUM bits require a "forming operation" of 100-1000 read/write cycles
- OUM write times have thermal limitations.
- - New materials for ICs. Understanding of material properties and control.
- Thermal isolation
- Near neighbor

- crosstalk.
- Electrode structure needs to be adapted/re-engineered for CMOS integration.

Molecular Manufacturing - Mechanical Nanocomputers

The Foresight Institute Nanotechnology pioneers Eric Drexler and Ralph Merkle have proposed and investigated, mechanical nanocomputers that would calculate using moving molecular-scale rods and rotating molecular-scale gears, spinning on shafts and bearings.

The researchers have focused on producing tiny machines and computers that would be assembled by the mechanical positioning of atoms or molecular building blocks one atom or molecule at a time, a process they term ``mechanosynthesis." This mechanical nanocomputer would operate like a nano-scale, complex programmable versions of an old-time mechanical calculator.

To date, most of the 'molecular manipulation' has been performed utilizing SPM techniques that are very slow and tedious, and are generally limited to two dimensions.

Research Needs

Unforeseen breakthrough of some sort is needed to make this technology reality.

C. Spin Orientation

Background

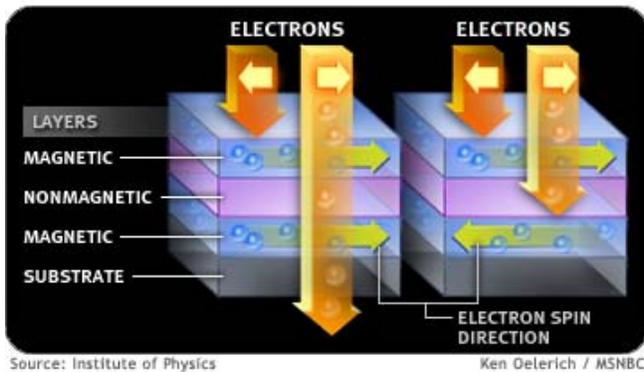
Spin or angular momentum of electrons or other subatomic particles hold promise for new computer and information transfer applications at both the individual or cumulative particle level. Spin states offer an attractive possibility of information transfer and storage that not only boost the performance of electronic devices, but also hold promise for lower power consumption as compared to traditional electronics. Spin has already been manifested in production electronic devices such as magnetic read heads, computer memory, and a multitude of sensors. The future of spin, however, is expected to lead to Single-spin transistor and storage applications. This relatively new field is called Spintronics (spin-electronics). In order to interface the outside world, Spintronics devices will probably need to interface other I/O technologies such as photonic, semiconductor, and/or magnetic devices and for most applications, all operating at room temperature.

The State Variable:

Just as positive/negative charge states can represent 0 and 1 computational states, electron spin with its two quantum spin states (-1: spin down, +1: spin up) can represent computational states. Computations are carried out by the interaction behavior between electrons using their spin coherent properties. Other spin mechanisms (proton, nuclear, etc) are also possible State Variables if they can represent, at a minimum, meta-stable computational states.

Specific Examples

There are many examples of spin-oriented devices in the literature such as:



Spin control

A giant magnetoresistance device consists of a three-layer sandwich of magnetic and nonmagnetic metal. When a current of spin-up and spin-down electrons is sent through the layers, electrons with the same spin pass through, but those with a different spin are scattered. If one layer's orientation can be changed by a magnetic field, then the device acts as a "spin valve," letting through more electrons when spins in the two layers are the same, as seen at left, and fewer when spins are different, as seen at right

Figure XXX Giant MagnetoResistance (GMR)

Spin-valve:

The Spin-valve (Transistor) is also illustrated in the above figure where the flow of electrons is modulated by the applied magnetic field.

Spintronics:

Spintronics refers to a general area of academic research involving coherent spin dependent transport, coherent state generation and detection and coherent coupling between photons, electrons and nuclei. It generally involves ferromagnetic semiconducting materials at liquid helium temperatures (5°K). It is an extremely rich area of investigation and holds great promise for the convergence of optics and electronics. It does not refer to any specific device at the present time.

Research Needs:

- I/O. interfacing the spin dependent logic device to the outside world
- Coherent spin transport across interfaces/materials, i.e., decoherence control
- Room temperature operation
- Scalability with manufacturing cost effectiveness, e.g., Silicon compatibility

D. Electric dipole orientation

Background

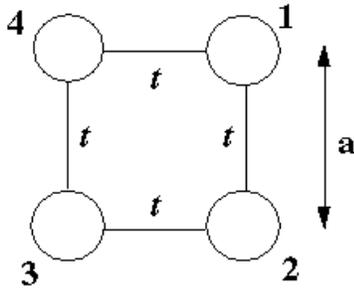
An electron pair possesses a vector dipole moment whose direction is defined by the straight line connecting the electrons. The vector orientation of an electron pair can therefore be used to store or manipulate information. The dynamics and energetics associated with manipulating the vector orientation of an electron pair is quite different from moving a single electron over or through a barrier and offers the potential for an alternative to MOSFET devices. The concept can be extended slightly to deal with pairs of quantum dots rather than individual electrons and since the net charge on a quantum dot can be of order 100, the noise problems associated with single electron devices are mitigated.

Typically, four quantum dots are fabricated in a lithographically defined quantum well structure called a cell that allows the net charge to distribute itself into one of two bistable states. One such cell configuration is a square with the quantum dots being located in each corner of the cell. The two bistable states¹ are realized when the net charge is evenly distributed between one of the two pairs of diagonal quantum dots.

¹ C. S. Lent et.al. "Bistable saturation in coupled quantum dots for quantum cellular automata", Applied Physics Letters, vol 62, pp 714-716, 1993.

The State Variable

The state variable is defined to be the geometrical orientation of the axis connecting the pair of charged quantum dots (QD). As mentioned previously, a square cell has bistable states and hence supports a binary data representation. A hexagonal cell with six quantum dots would support a base 3 data representation, etc. The state variable will be toggled if the net charge migrates from one diagonal QD pair to the other diagonal QD pair. External electric fields from gates or adjacent cells will cause such a charge migration and provide the basis for manipulating the state variable.



Specific Examples

Quantum Cellular Automata² (QCA) systems have been proposed, analyzed and fabricated based on electric dipole orientation as the state variable. The basic cell structure of such QCA systems is shown in the figure at left. The electric charge is distributed between QDs 1-3 or QDs 2-4 to form the two bistable ground states. Tunnel barriers separate the individual QDs.

In principle QCA devices can have switching energies several orders of magnitude smaller than CMOS devices but many practical problems prevent this from being realized in practice such as a requirement of mK temperatures to exceed the thermal noise limit. Additional problems include lack of gain, asynchronous operation, lack of input/output

isolation and existence of metastable states resulting in system lockup.

The architecture configuration supports nearest neighbor communication rather than global point-to-point interconnects. This is a potential advantage but would require massive changes in manufacturing technology which and very difficult to justify.

Research needs

- Substrate power delivery to the QCA cells
- High precision manufacturing techniques
- Readout devices for dipole orientation

E. Photon Intensity

Background:

Information storage and computation using photons is an attractive area for investigation. The high speed and thus subsequent high information capacity of photons hold a lot of promise. So far, the progress in the use of photon intensity for highly integrated computations is limited due to configuration (e.g. component size and photon size) as well as the lack of compatibility with CMOS processes for continued scalability. Computations using photons hold promise also in massively parallel information processing, such as done in holographic-based demonstrations. A few of the apparent challenges lie in the integration of photonic devices with CMOS, the interface between electrical signals and photonic signals, miniaturization, and power consumption.

The State Variable:

Computational states can be represented by photon intensity, in binary logic (low as 0, high as 1), multi-level logic and even analog representations. Interaction through interference of photons realized via reflection or deflection by controlled objects and switching or modulating by nonlinear optical or electro-optical materials can be used to carry out computations.

² C.S. Lent et al. al., "Quantum Cellular Automata", Nanotechnology, vol. 4, pp. 49-57, 1993.

Specific Examples

There are many examples of devices using photon intensity in the literature such as:

Free-space interference devices:

- Holographic arrangements
- Spatial light modulators (DLP, MEMS, etc...)

Optical Fiber and Hybrid Semiconductor-Fiber devices:

Single or multi-arm interferometric architectures – nonlinearities in fiber or semiconductor material are used for the ultra fast interference mechanism, such as:

- Nonlinear Optical Loop Mirror (NOLM)
- Terahertz Optical Asymmetric Demultiplexer (TOAD)
- Ultra fast Nonlinear Interferometer (UNI)
- SLALOM, etc.

Waveguide devices:

Compact single or multi-arm interferometric architectures such as:

- Mach-Zehnder Interferometers
- Multi-mode Interference couplers
- Multi-arm interferometers incorporating nonlinear elements.

Electro-optical interface:

Example:

- LiNbO₃ modulator – typically used for 10+ Gbps optical modulation (very rapid material changes), but tends to be power hungry (5V swing).

Research Needs:

Research needs are believed to primarily fall into following general areas although others may be identified:

- I/O mechanisms, such as electromechanical modulation using micro mirrors, optical/electrical conversion, and energy efficiency
- Non-linear optical material for conversion / interaction efficiency
- Scalability of on-chip applications

F. Quantum state

Background

Quantum computing is being studied as a means of achieving exponential speedups relative to conventional computers on a few specialized algorithms such as sorting and cryptographic encoding. The speed up derives from the ability to manipulate the large amounts of data stored in a single quantum state in parallel.

The quantum state of an arbitrary quantum system is defined to be an N dimensional vector in Hilbert space. Most quantum computer concepts are built on a specialized two dimensional quantum system called a quantum bit or Qbit. The quantum state ψ of such a binary system may be written as shown in the following equation.

$$|\Psi\rangle$$

$|0\rangle$ and $|1\rangle$ are basis states

The constants a and b completely define the quantum state ψ in terms of the basis states $|0\rangle$ and $|1\rangle$. The state is said to be coherent as long as the constants that define the state do not change. In practice, no quantum system can be completely isolated from its environment and the amount of environmental

coupling is measured as decoherence time. Experimental decoherence of various Qbit representations range from 10^{-1} to 10^{-9} seconds. Physical representations with only 2 allowed basis states are desirable.

In order to be useful for information processing, any physical representation of quantum state must meet four requirements.

1. The quantum state must be robust – it must maintain its coherence long enough to perform a useful number of quantum operations
2. It must be possible to prepare an initial optical state
3. It must be possible to manipulate the quantum state in deterministic ways through external means
4. It must be possible to read out the optical state.

Specific example

Phosphorus 31 atoms embedded in a silicon lattice have been proposed by Kane³ et. al. as an ideal qubit for storing quantum state and are the subject of intense research activity aimed at developing a solid state quantum computer. The spin of the valence electron of the ³¹P atom can exist in the superposition of states described above and function as a single Qubit with additional ³¹P atoms implanted at adjacent lattice sites functioning as additional Qubits. A silicon lattice makes a preferred host because the predominant naturally occurring isotope is ²⁸Si, which has zero nuclear spin and hence reduces decoherence effects. A gate electrode positioned between Qubits can manipulate the wavefunctions of the valence electrons so they overlap and become entangled. Initial states of the Qubits can be prepared by using Electron Spin Resonance to flip the spins of individual valence electrons and place them in the desired initial configuration. Results can be read out from individual Qubits by standard atomic spectrographic techniques, which yield the spin up/ spin down state of the electron at the conclusion of the calculation.

Research needs

- Control of quantum decoherence effects –isolation from environment
- Techniques to manipulate quantum state
- Techniques to read out quantum state –ultra-sensitive techniques capable of detecting a single electron spin
- Techniques to prepare an initial quantum state –e.g. imprinting photon polarization on to electron spin state

G. Molecular state

Molecular state is perhaps the most ambiguous and difficult to define of the alternative state variables being addressed in this document. This is due to the fact that many proposed research devices use particular electrical, mechanical, chemical and photonic characteristics of particular molecular structures to accomplish a wide variety of information processing tasks. However, their molecular state is constant and hence they do not store or manipulate information in their internal molecular structure. Within the context of this taxonomy, only devices that store or manipulate information based on molecular state are considered to be molecular state devices.

There exist three main technological areas within ME, organic electronics, nanotube devices, and single molecule devices. Organic electronics include OLED type devices, large area organic FETs, and organic thin film technologies. Nanotube devices are predictably, devices made from nanotubes. These may include nanotube sensors, FETs, emission devices, NEMS, thermal management devices, and low-K films. Finally, single molecule electronics are technologies that utilize a single molecule as a switching device. This technology is seen as being more 'far horizon' technology, but with an extraordinary potential of fast switching times (comparable with Si CMOS technology), cheap production costs, small form factor,

³ Kane, Bruce, A silicon based nuclear spin quantum computer. *Nature*, 393:133-137,1998.

very low energy consumption/heat generation and added functionality through integration with organic systems.

Currently in the area of molecular electronics, we can produce billions of devices/transistors very cheaply in a beaker. We can tailor these molecular devices, through chemical synthesis, to be electronic, optical or even mechanical devices. The limiting factor at present to this technological dream becoming a reality is the ability to self assemble these devices in the proper configuration to produce a useful system. If this could be achieved, the possibilities are enormous.

Change in molecule physical structure

The marriage of conventional CMOS devices with molecular monolayers is becoming a very attractive arena for university research, specifically as a methodology for communication of the CMOS component to the outside world through sensor applications. Generally, the sensor consists of polarizable molecular monolayers that adhere (i.e. self-assemble) to an underlying CMOS-compatible integrated circuit. The molecular monolayers are designed in such a way that their physical structure changes after exposure to the chemical of interest. The change in physical structure leads to a change in their electrical polarization, which is detected by a sensitive transistor immediately below the monolayer. It is possible to design the molecular monolayers to respond to a wide range of individual chemical agents. The device combines the enormous flexibility associated with organic synthesis with the mass production capability of silicon chips.

Change in molecule internal structure, resulting in a change in HOMO-LUMO states. NDR devices.

Recent work at Yale and Rice Universities illustrate a molecular system consisting of thousands of molecules showing an impressive NDR peak to valley ratio of 1000:1. These results are impressive when you consider that the molecules were only chemically contacted to the bottom electrode in the experimental set-up. The top contact was a physical contact between the Ti and the molecule.

REDOX Mechanisms within a molecule (variation of electronic charge)– E.g. PANI (polyaniline)

The use of a REDOX system to act as a switching mechanism is probably the closest and most promising molecular performer to current silicon technology.

Molecular devices give high density, non-volatility for memory apps. Molecular devices are generally very biologically compatible. Many sensor applications possible.

Research needs

- Stability of molecular 'sensing' layer. Reversible, reusable?
- Development of sensor molecules, and subsequent attachment to CMOS IC. Contacts!

H. Phase Logic Section

Introduction

The concept of Phase Logic, as originally proposed independently by von Neumann and Goto, represents logic states in terms of temporal (or phase) differences between a sub-harmonic logic signal and a synchronized ac power supply or sub-harmonic pump. In a binary logic system, the two logic states of the output signal may have phase states separated by π and are synchronized to the phase of the ac generator. This is contrasted with the conventional representation of logic states in CMOS by voltage levels.

Technological Approaches

In one scheme for Phase Logic, von Neumann proposed using a threshold-based non-linear element, or a Parametron, to combine an input logic sinusoidal signal with the pump signal to create an output logic signal. The frequency of this output signal is a sub-harmonic of the pump and its phase is determined by the input logic signal. The frequency of the pump is a harmonic multiple of the frequency of the input logic signal. For the case of binary logic the pump frequency is twice that of the input logic signal, and the two logic states are represented by a phase difference of 0 and π radians. Higher order multi-valued logic of order n can be realized using a pump whose frequency a multiple of n times the frequency of the input signal.

In a second scheme for Phase Logic, referred to as Tunneling Phase Logic (TPL), Kiehl proposes use of the single-electron tunneling (SET) effect to realize a binary phase-state representation of logic signals. He proposes use of an ultra-small tunnel junction to realize voltage oscillations at the frequency $\frac{1}{\tau_{\text{set}}}$ when biased with a constant current, I , injected into one terminal of the tunnel junction. Governed by the Coulomb Blockade Effect, this phenomenon allows the voltage on the small tunnel junction to increase linearly until a single electron tunnels across the junction. This tunneling event first causes the voltage to drop precipitously followed by the next cycle of linear increase and the next tunneling event. The phase of this voltage oscillation is synchronized globally across a 2D-lattice array of these tunnel junctions using an ac pump connected to the opposite terminal of the 2-terminal tunnel junction. The frequency of this pump is $2\frac{1}{\tau_{\text{set}}}$. The phase of the tunneling event is indeterminate between two possible phases or states because of the $2x$ harmonic difference between the frequencies of the voltage oscillation and the pump. A particular phase of the voltage oscillation (of the two possible phases) can be selected by an input signal possessing that phase and capacitively coupled to the current-driven node of the tunnel junction. Thus the phase of one "gate" or tunnel junction can select or set the phase of an adjacent gate, thus transferring a logic state from one tunnel junction gate to the next.

Architectural Approaches

Several architectural approaches to realizing general computer functions have been proposed for both of these approaches to Phase Logic. These approaches range from majority logic used to represent Boolean functions to distributed processing functions exploiting highly non-linear coupling between nearest neighbor (locally connected) TPL cells. Most suitable to Von Neumann's approach to Phase Logic, a gate in majority logic consists of an odd number of summed multiple inputs controlling a single output. The output is simply a function of the sum of the majority of the inputs, with phase cancellation of the inputs being the operative mechanism. Tunneling Phase Logic, being a 2D-lattice array of non-linearly coupled nearest-neighbor (locally connected) tunnel junctions, offers an abundant array of possible information processing architectures. These architectures include distributed Neural Networks using integrate-and-fire threshold elements and locally interconnected Cellular Nonlinear Networks that can be used for image processing and extended to realizing generalized arbitrary Boolean functions.

This section will outline research needs associated with Phase Logic, including both the nano-scale materials and device science and technology together with the information processing architectural and systems.

Research Needs and Opportunities

Research needs and opportunities related to Phase Logic can be separated into the two categories of technological and architectural. As discussed above, two technological approaches to realizing Phase Logic are the Parametron and Tunneling Phase Logic using single electron tunnel junctions. Architectural approaches to the use of Phase Logic in information processing include Majority Logic and Cellular Nonlinear Networks.

Challenges gating application together with specific research needs and opportunities related to these technological and architectural areas are outlined below. In general, the Parametron requires tuned resonant circuits to support the oscillations and power transfer between pump and sub-harmonic signal frequencies. Consequently, the time delay required for sub-harmonic oscillation increase in the resonant circuit of a parametron can be many cycles, thus causing the phase locking of the output signal in response to the input to take much longer than one period of the sub-harmonic of the pump generator.

Further, application of the Parametron to Majority Logic is based on cancellation of input signals, whose phase is separated by p radians, to determine the logic state. Adequate cancellation requires uniformity in the signal amplitude, which depends on the saturation mechanism that, in turn, is related to careful control of several circuit parameters. In the operation of a parametron circuit, the stages are clocked by modulating the amplitude of the pump generator. The logic flow in a parametron circuits requires three or more clock signals, each with a different phase. Thus three or more modulated and coherent microwave signals will need to be distributed throughout the circuit to obtain proper logic flow.

Tunneling Phase Logic operating at room temperature requires a two dimensional periodic array of single electron tunnel junctions. These junctions would be composed of floating metallic nodes or islands of extremely small dimensions (0.6-nm) to realize the extremely small capacitances (0.06-aF) needed to provide single electron tunneling governed by the Coulomb Blockade effect. Further, the floating metallic nodes must be isolated from their environment by extremely scaled, high-value resistances, exceeding $26 K\Omega$, and must deal with their substantial sensitivity to background charges.

Of the two architectural approaches discussed above, majority binary or multi-valued logic and cellular non-linear networks (CNN), only CNN combined with TPL appears to offer a completely new paradigm for information processing that is both locally connected yet spatially distributed. The principle research needs related to the CNN paradigm is to explore the extent that TPL/CNN can be applied to perform generalized computation and information processing functions. In a simpler form, CNN/TPL has been shown to perform highly parallelized image processing functions. However, application of more generalized information processing functions requires new algorithms and techniques for solving large sets of non-linear equations. Some specific research needs related to TPL/CNN are shown below.

Research needs

- Algorithms and applications for TPL/CNN.
- Circuit and system architectures for TPL/CNN
- Input/output schemes for TPL/CNN information processing system. (For example, optical inputs)
- Physical mechanisms and structures, other than TPL, to realize integrate-and-fire neuron-like devices for CNN architecture.